Electronic Version
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Back Gate FinFET SRAM

Abstract

A compact semiconductor structure having back gate(s) for controlling threshold voltages and associated method of formation is disclosed. Fabrication of the semiconductor structure starts with a semiconductor region formed directly on an underlying electrically isolating layer. Then, a mandrel and a spacer are formed on the semiconductor region. Next, a back gate region is formed separated from the semiconductor region by a back gate isolating layer and covered by an inter-gate isolating layer. Next, a portion of the semiconductor region beneath the mandrel is removed so as to form an active region adjacent to the removed portion of the semiconductor region. Finally, a main gate region is formed in place of the removed portion of the semiconductor region and on the inter-gate isolating layer. The main gate region is separated from the active region by a main gate isolating layer and separated from the back gate region by the inter-gate isolating layer.